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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,004	02/08/2002	Woo Young So	1514.1010	6442
49455	7590	12/15/2005	EXAMINER	
STEIN, MCEWEN & BUI, LLP 1400 EYE STREET, NW SUITE 300 WASHINGTON, DC 20005				SEFER, AHMED N
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/068,004	SO ET AL.	
	<b>Examiner</b> A. Sefer	<b>Art Unit</b> 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### **Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 29 September 2005.

2a)  This action is **FINAL**.                            2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## **Disposition of Claims**

4)  Claim(s) 12, 14-16, 22 and 24-27 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 12, 14-16, 22 and 24-27 is/are rejected.

7)  Claim(s) \_\_\_\_\_ is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on \_\_\_\_\_ is/are: a)  accepted or b)  objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All    b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date .

4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_ .

5)  Notice of Informal Patent Application (PTO-152)

6)  Other: \_\_\_\_ .

## **DETAILED ACTION**

### ***Response to Amendment***

1. The amendment filed September 29, 2005 has been entered; new claims 26 and 27 have entered.

### ***Specification***

2. Claim 12 is objected to because of the following informalities: Since the low-density source and drain regions and lightly doped drain (LDD) regions one and the same, the recitation calling for “low-density source and drain regions having a same conductivity as high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high density source and drain regions, wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers,” is redundant and confusing. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 12, 15, 16 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. (“Lee”) USPN 6,549,252.

Lee discloses in figs. 3-5 a thin film transistor (TFT), comprising: a substrate; a semiconductor layer 72 formed over said substrate having end portions; a first insulating layer 74

disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer; a gate electrode 76 formed over said first insulating layer; a capping layer (upper portion of region 80) formed over said gate electrode; spacers (portions of region 80 on both sidewall portions of gate electrode 76) formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer; high-density source and drain regions 92 formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers, the high-density source and drain regions spaced apart from the gate electrode and the capping layer; low-density source and drain regions 90 having a same conductivity as high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high density source and drain regions, wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers; and source and drain electrodes (col. 7, lines 23 and 24) which directly contact, respectively, and without contact holes (col. 7, lines 31 and 32), said high density source and drain regions.

Regarding claim 15, Lee discloses (cols. 6 and 7, lines 55-67 and 33-35 respectively) a silicide layer or refractory metal (as in claim 16) formed between said source electrode and said high-density source region and between said drain electrode and said high-density drain region.

Regarding claim 26, Lee discloses high density source and drain regions and low-density source and drain regions extending through the entire thickness of said semiconductor layer.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. ("Chang") US PG-Pub 2002/0153527 in view of Yamazaki et al. ("Yamazaki") USPN 5,568,288.

Chang discloses in figs. 1A-1F a thin film transistor (TFT), comprising: a substrate; a semiconductor layer 102 formed over said substrate having end portions; a first insulating layer 104 disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer; a gate electrode 108 formed over said first insulating layer; a capping layer (upper portion of region 114) formed over said gate electrode; spacers (portions of region 114 on both sidewall portions of gate electrode 76) formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer; high-density source and drain regions 116 formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers, the high-density source and drain regions spaced apart from the gate electrode and the capping layer; low-density source and drain regions 110 having a same conductivity as high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high density source and drain regions, wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers, but lacks anticipation of source and drain electrodes contacting high density source and drain regions without contact holes.

Yamazaki discloses in figs. 21 and 22 a thin film transistor (TFT), comprising: a substrate; a semiconductor layer formed over said substrate having end portions; a gate electrode

107 formed over an insulating layer 103; and source and drain electrodes 102 which directly contact, respectively, and without contact holes, high density source and drain regions 104/105.

Therefore, in view of Yamazaki, one having ordinary skill in the art at the time the invention was made would be motivated to modify Chang's device by incorporating the teachings of Yamazaki so as to complete the thin film transistor as taught by Yamazaki.

Regarding claim 14, Chang discloses (Pars. 0029 and 0032) said first insulating layer, said capping layer and said spacer are of an oxide.

7. Claims 22, 24 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda et al. ("Yoneda") USPN 5,837,568 in view of Lee.

Yoneda discloses in figs. 12 and 13 an active matrix display device, comprising: a substrate 10; a semiconductor layer having end portions formed over said substrate; a first insulating layer 12 formed over said semiconductor layer so as to expose portions of said semiconductor layer; a gate electrode 13 formed over said first insulating layer; a capping layer 14 formed over said gate electrode; spacers 15 formed over said first insulating layer and on side wall portions of said gate electrode and said capping layer; high-density source and drain regions 11 formed at the ones of the end portions of said semiconductor layer; low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at off-set regions of said semiconductor layer partially under said spacers so as to have said semiconductor layer with lightly doped drain (LDD) regions partially under said spacers; source and drain electrodes 17/18 which directly contact, respectively, said high density source and drain regions; a planarization layer 19 having an opening portion CT3 which exposes a portion of one of said source and drain electrodes; and a pixel electrode 20 formed on the planarization

layer, the pixel electrode contacting one of the second source and drain electrodes through the opening portion, but lacks anticipation of a first insulating layer formed over said semiconductor layer so as to expose ones of end portions of said semiconductor layer and source and drain electrodes contacting high density source and drain regions without contact holes.

Lee discloses in figs. 3-5 a thin film transistor (TFT), comprising: a substrate; a semiconductor layer 72 formed over said substrate having end portions; a first insulating layer 74 disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer; a gate electrode 76 formed over said first insulating layer; spacers (portions of region 80 on both sidewall portions of gate electrode 76); high-density source and drain regions 92 formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers; low-density source and drain regions 90 having a same conductivity as high-density source and drain regions formed at off-set regions of said semiconductor layer under said spacers so as to have said semiconductor layer with lightly doped drain (LDD) regions under said spacers; and source and drain electrodes (col. 7, lines 23 and 24) which directly contact, respectively, and without contact holes (col. 7, lines 31 and 32), said high density source and drain regions.

Therefore, in view of Lee, one having ordinary skill in the art at the time the invention was made would be motivated to modify Yoneda's device by incorporating source and drain electrodes, which directly contact, respectively, and without contact holes, said high density source and drain regions since that would simplify the process as taught by Lee.

Regarding claim 24, Lee discloses (cols. 6 and 7, lines 55-67 and 33-35 respectively) a silicide layer formed between said source electrode and said high-density source region and between said drain electrode and said high-density drain region.

Regarding claim 27, Lee discloses high density source and drain regions and low-density source and drain regions extending through the entire thickness of said semiconductor layer.

8. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Lee as applied to claim 22 above, and further in view of Yamazaki et al. US PG-Pub 2003/0207502 ("Yamazaki '502").

The combined references disclose the device structure as recited in the claim, but lack anticipation of an organic electro-luminescence (EL) layer.

Yamazaki '502 discloses (pars. 0279 and 0343 and fig. 25) an organic electro-luminescence (EL) layer 4029 and a cathode electrode 4030 sequentially formed on a first predetermined area of a pixel electrode and on a second predetermined area of a planarization layer 4142.

Therefore, in view of Yamazaki '502, one having ordinary skill in the art at the time the invention was made would be motivated to modify the device by incorporating the teachings of Yamazaki '502 so as to display bright images as taught by Yamazaki '502.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LATHAN J. FLINN  
DISPOSITIONARY PATENT EXAMINER  
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ANS  
December 6, 2005